

Superior AVC HD Encoder Architecture

Single-slice AVC encoder sets an unprecedented benchmark in HD video quality at relatively low bit rates

Executive Overview

As service providers in the broadcast industry face unprecedented competition for viewers, new encoding technology can be deployed to deliver more content over existing bandwidth to deliver the new, advanced services consumers are demanding. A technologically superior implementation by Scientific Atlanta of the MPEG-4/H.264 advanced video compression (AVC) encoding standard will enable service providers to take advantage of bandwidth savings while delivering the high-quality video experience that high-definition television (HDTV) demands through the implementation of single-slice AVC encoding.

Introduction

The analog-to-digital migration for broadcast video content production and distribution is underway, with digital content rapidly replacing the analog format that has enjoyed widespread popularity and use for decades. The transition is fueled by the digital environment's flexibility in handling video content at all stages from production to transport/storage to decoding/display. The infrastructure needed to enable this digital transformation is being put in place at a rapid pace, allowing both content providers and service providers to potentially expand their market reach over the next few years.

Service providers in the broadcast industry face unprecedented competition for viewers. In a landscape that was previously dominated by the cable and satellite industries, IP Television (IPTV) companies are now competing for the same customers using their Digital Subscriber Line (DSL) infrastructure. The competitive landscape is driving service providers to develop ways to differentiate their services and to adopt new solutions for the encoding and delivery of digital video. Customers would like to receive more channels for a given service, creating the need for a more efficient use of existing bandwidth. At the same time, they are becoming more demanding in terms of the video quality they expect to see on their TVs, requiring broadcasters to implement sophisticated video pre-processing technology. Despite their increasing concern for competitive services and video quality requirements, customers also still demand that the cost of service be as low as possible. Therefore, companies such as Scientific Atlanta, a Cisco company, have been developing advanced pre-processing and compression solutions for the most efficient delivery of high-quality digital video.

For more than a decade, compression solutions have been based on a standard developed by the Moving Pictures Experts Group (MPEG), known as MPEG-2 video, which has been the visual coding standard of choice for the broadcast video industry. The standard operates at bit rates from around 3 to 6 Mbps for standard-definition (SD) resolution and from around 12 to 20 Mbps for high-definition (HD) resolution. The MPEG-4/H.264 Advanced Video Compression (AVC) encoding standard, however, is revolutionizing the broadcast industry by presenting a viable alternative to MPEG-2 video. AVC allows encoders to achieve more than 50 percent savings in bandwidth compared to MPEG-2 compression, hence its strong value proposition. In fact, AVC has now enabled a substantial market shift, allowing IPTV service providers to become much more competitive in providing both SD and HD video services over their networks.

However, AVC is also a substantially more complex standard than MPEG-2 video, and both the AVC encoders and decoders are much more demanding in terms of computations and memory than their MPEG-2 counterparts. This, coupled with the fact that HD video requires the processing of six times as many pixels as SD video, makes the development of a high-quality AVC HD encoder a daunting task. In fact, most companies are forced to split the picture into either three or six slices in order to reduce the computational and memory transfer requirements. Unfortunately, this yields a reduction in video quality due to the less efficient Context-Adaptive Binary Arithmetic Coding (CABAC) encoding and the constraints imposed on the encoding algorithms such as de-blocking (loop) filtering, motion estimation and rate control.

Despite these challenges, at the 2006 National Association of Broadcasters (NAB) conference Scientific Atlanta was able to demonstrate the first single-slice (i.e. one slice per picture) AVC encoder, setting an unprecedented benchmark in HD video quality at relatively low bit rates such as 7 Mbps and 8.5 Mbps. The new encoder is based on a scalable AVC HD architecture that provides huge horsepower to implement the full set of AVC High Profile (HP) features as well as all of Scientific Atlanta's optimized video pre-processing and compression algorithms. Due to its scalability and unique Printed Circuit Board (PCB) layout, the new Scientific Atlanta HD architecture also allows future video quality enhancements through mostly short-term software up-grades (i.e. by downloading new DSP/FPGA code) and also long-term hardware upgrades (e.g. by replacing cards with others using better and/or more powerful devices).

In what follows, we describe the HD architecture and highlight its two major benefits: 1) Superior HD video quality and 2) Maximum flexibility for future quality enhancements through software and hardware upgrades.

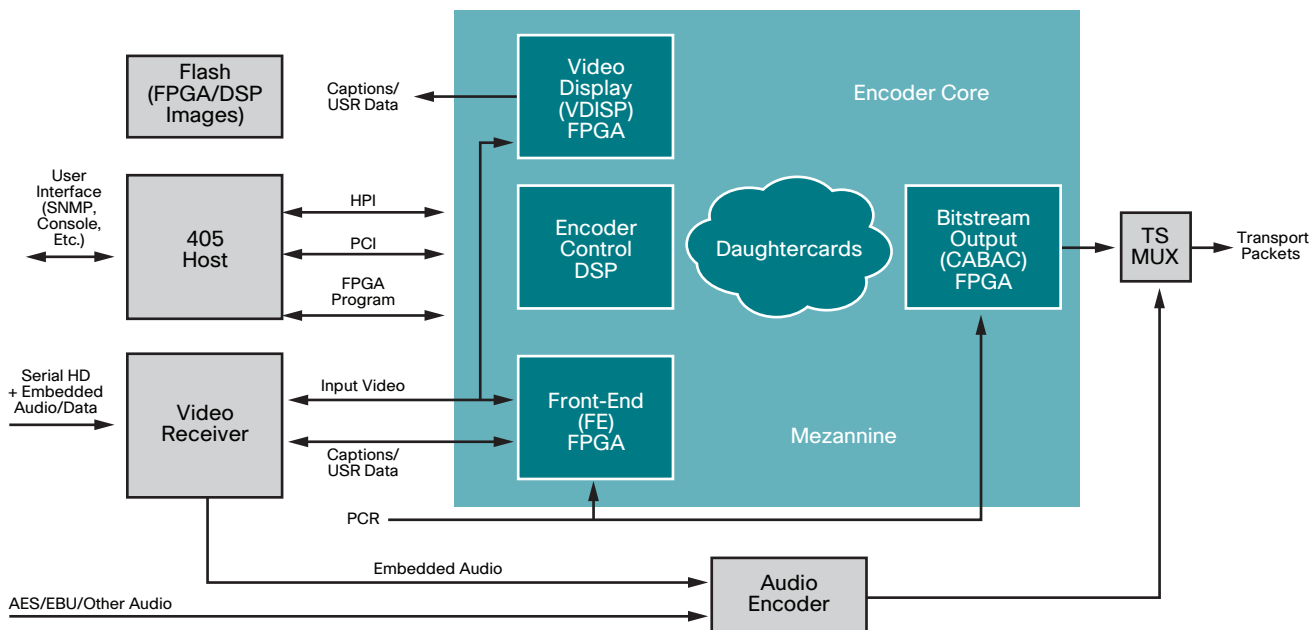
Overview of the Scientific Atlanta HD Encoder Architecture

The HD encoder product is designed to support resolutions up to 1080i30 and bit rates up to 25 Mbit/s. To achieve the best possible video quality, the HD encoder employs extensive pre-analysis, truly full intra/inter search and advanced rate control. But perhaps most beneficial to video quality is the encoder's use of a single-slice per picture to avoid transition artifacts.

Given the huge amount of data needed to represent HD video and the requirement for a single-slice HD architecture, many dedicated Field Programmable Gate Arrays (FPGAs) are used to perform all of the "heavy lifting" functions, while Digital Signal Processors (DSPs) perform the key decisions in functions such as pre-analysis, rate control and coding mode selection.

As shown in Figure 1, the HD encoder consists of an encoding core, which includes multiple sub modules based on DSPs and FPGAs that perform the bulk of the H.264 encoding process reside.

Figure 1. High-Level Description of the Scientific Atlanta AVC HD Encoder Core



As shown in Figure 2, each of the sub modules performs a certain function of the core video encoder. The Pre-Analysis (PA) card implements all of the pre-analysis algorithms, which produce scene complexity measures, as well as macroblock (MB) bit production and motion vector estimates, needed for Group-Of-Pictures (GOP) selection, motion estimation and rate control. Two additional cards perform extensive full-pel and sub-pel motion search, and the refined full-resolution motion vector estimates are communicated to a Mode Decision (MD) block, which determines whether the subject macroblock should be skipped, intra-coded or inter-coded (i.e. through motion-compensated prediction). The MD card also performs the reconstruction of the luminance pixels once the mode decision process is completed. Finally, the Loop-Filter-Chrominance (LFC) block implements the reconstruction of the chrominance pixels and the MPRG-4 de-blocking (loop) filtering of the luminance and chrominance reconstructed pixels. Finally, the PA block is used to implement our pre-filtering system as well as the Picture-in-Picture (PIP) feature.

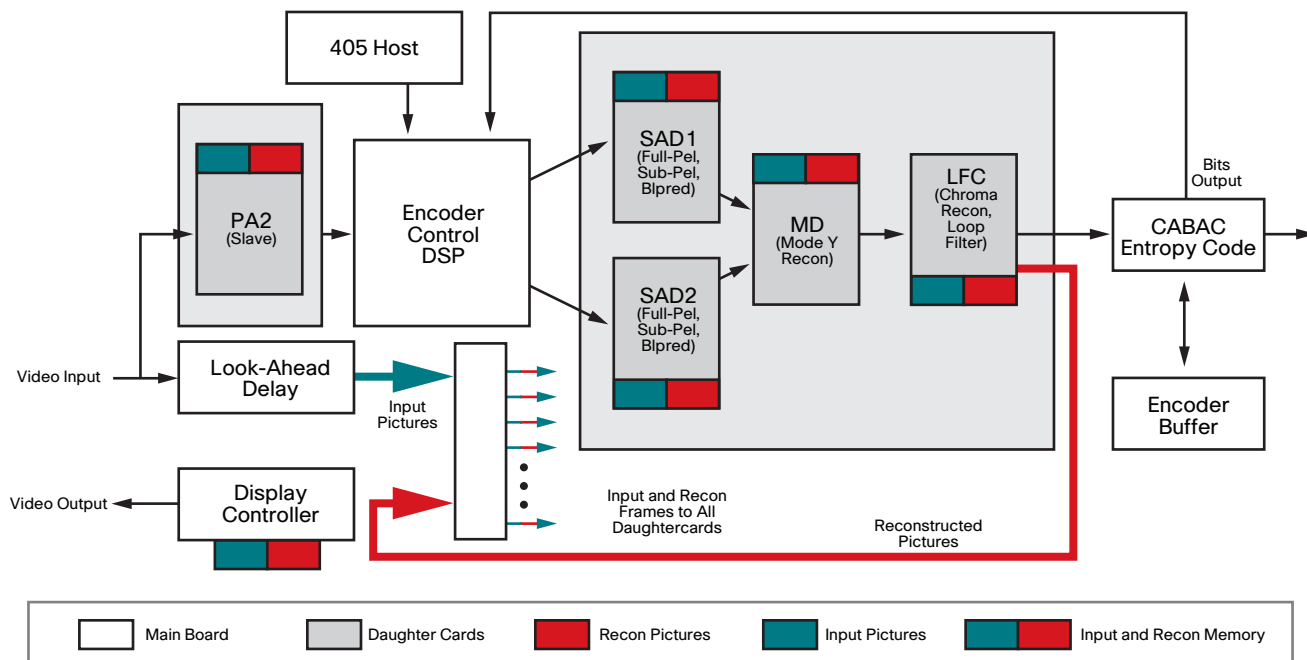
What Makes the Scientific Atlanta AVC HD Encoder Architecture Superior?

The HD architecture enables our unique single-slice HD encoder to deliver unmatched AVC HD video encoding to the market, resulting in superior video quality, as well as higher flexibility, performance, reliability and efficiency, as compared to existing AVC HD video encoders.

Video Quality

When developing the HD architecture, the objective was to superior video quality at all times. In order for video quality never to be compromised, the HD architecture provides unprecedented horsepower to implement (1) the full set of features of the AVC HP standard, (2) advanced pre-processing algorithms, (3) extensive intra and inter (motion) search, and (4) sophisticated rate control, all without splitting the picture into multiple slices during the video encoding process.

Figure 2. Overview of the Scientific Atlanta AVC HD Encoder Architecture



The AVC HP standard supports many features that enable compliant encoders to achieve very high coding efficiency. Such features include quarter-pel resolution motion estimation and compensation with multiple block sizes and reference frames, multiple-mode 4x4, 8x8 and 16x16 intra prediction and compensation, video-adaptive de-blocking (loop) filtering, adaptive 4x4/8x8 integer transformation, advanced non-uniform quantization, and super-efficient CABAC. Other important features include quantization scaling and weighted prediction, which are designed to maximize subjective quality. All features, while often demanding in computation and memory requirements, are required to deliver the best possible video quality for various types of video content and bit rates.

The advanced pre-processing algorithms include powerful noise reduction techniques collectively referred to as *PreSightPlus*, as well as multi-pass look-ahead spatio-temporal analysis methods. The spatial analysis methods involve the computation of spatial activity measures for frame/field coding decision, prediction of bit rate, etc. The temporal analysis methods, which involve the computation of motion activity measures, are used for prediction of bit rate, detection of scene changes, detection of fades, etc.

The HD encoder selects one intra-coding mode for the luminance part of an MB from four 16x16, nine 8x8 and nine 4x4 intra coding modes. It also selects one intra coding mode for the chrominance component of an MB from four 8x8 intra coding modes. Moreover, the HD encoder performs a three-stage hierarchical motion search, with an adaptive search window size and a motion search range up to 580 x 272.

The HD encoder also performs both high- and low-level rate control to guarantee stable Constant-Bit-Rate (CBR) and capped Variable-Bit-Rate (VBR) operations in an IPTV system, while maintaining consistently high video quality. The high-level rate control takes into account the target bit rate and the scene complexity results of the pre-analysis sub-system to distribute the bits among the various pictures of the subject GOP and determine an average quantization value for each picture, among other operations. The low-level rate control module is a complex MB-adaptive rate control system that maximizes subjective quality using locally computed spatio-temporal complexity measures.

The HD encoder performs all of these complex operations following a single-slice coding approach. In other words, unlike other AVC HD encoders, the Scientific Atlanta HD encoder does not split the picture into multiple slices for subsequent encoding. This single-slice HD encoding architecture yields significantly better video quality than that achieved by multiple-slice HD architectures, for many reasons. First, rate control is inherently more effective because it will have easy access to the statistics of the whole picture. Second, not having to re-set statistics at the beginning of each slice within a picture will maintain high CABAC efficiency. In addition, loop filtering, which cannot be applied across multiple slice boundaries, will be applied to the full picture, significantly reducing blocking artifacts. Last, but not least, the Scientific Atlanta HD encoder will not have to perform motion compensation across slice boundaries, needed to avoid unnecessary blocking artifacts that would have been generated when two parts (one in each slice) of an object are motion-compensated differently. Obviously, motion compensation across slices would require additional complexity and memory transfer overhead.

To implement the entire AVC complex encoding algorithms in real-time without splitting the picture into slices, the Scientific Atlanta HD architecture provides incredible horsepower, including specifically four Texas Instruments 1 Ghz C6415 DSPs and multiple Xilinx Virtex 4/60 FPGAs, through an FPGA-based design that delivers not only the maximum number of operations per second but also the fastest data flow. Table 1, which presents execution performance numbers and current loading percentages for some of the encoder sub-systems, demonstrates the advantages of the Scientific Atlanta FPGA-based design. Note, for example, that the devices used for full-pel search perform 190 billion Sum-of-Absolute-Differences (SADs) per second. This is obviously more powerful than four TI 1 Ghz C6415 DSPs, which would theoretically provide a peak rate of only 32 billion pixel operations per second. Moreover, note that across the various Xilinx FPGAs, there is an astonishing 80 Gigabyte/second peak external memory bandwidth available to the various processors. Between the FPGAs, a network of multi-gigabit links provides roughly 160 GBit/s bandwidth, enabling all of the real-time data communication required by the single-slice HD encoder. On the other hand, each of the TI C6415 DSPs has only 1-GByte/s peak I/O bandwidth, which must be shared between memory and other processor data exchanges, impacting negatively parallelism.

Table 1. Performance and Loading of the Devices in the Encoder Sub-Systems

Sub-System	Performance
Full-Pel Motion Search	190 Billion Pixel SADs/second
Sub-Pel Motion Search	1 Billion Pixel SADs/second + 1 Billion Ops/second for ¼ Pel Interpolation
Mode Decision	250,000 Macroblocks/second
Pre-Analysis	N/A

Table 1 also illustrates the current calculating capacity of the encoder. This, coupled with the fact that many of the FPGAs have still not been used, demonstrates that there is abundant processing room for future quality enhancements over many years.

Flexibility

Despite it being hardware-based, the Scientific Atlanta HD architecture provides maximum flexibility for future quality enhancements through mostly software upgrades but also hardware upgrades. Software upgrades can be performed through new DSP/FPGA software implementing quality enhancement features.

DSPs, which perform all key decisions and implement the most intelligent features, can be easily re-programmed as better coding decisions and more sophisticated high- and low-level rate control algorithms are developed. In fact, since both the rate-control and pre-analysis DSPs are currently less than 65 percent full, more effective algorithms can be added to improve both coding decisions and rate control. FPGAs, which perform all of the remaining tasks, can also be re-programmed to implement new algorithms and features toward more advanced spatio-temporal pre-analysis, more effective motion-compensated prediction and more accurate rate/quality mode selection. As shown in Table 1, the average percentage loading for some sub-systems on the Xilinx FPGAs varies from as little as 33 percent (with two un-used FPGAs) to as high as 75 percent, leaving abundant room for the addition of features and algorithms targeting higher subjective video quality.

Hardware upgrades can also be easily performed due to the architecture's modular PCB design, which employs many cards with a few devices. In fact, the architecture allows the simple replacement of cards with others containing more powerful hardware (e.g. higher-density FPGAs), that will be needed to implement long-term product enhancements.

Other Advantages

Unlike existing software encoders, this hardware-based Scientific Atlanta HD encoder achieves repeatable and predictable performance levels regardless of video content or system loading. Moreover, the HD encoder is very reliable since it employs redundant power supplies, it uses no hard disk drives and it is immune to PC viruses. Last but not least, the HD encoder is light and efficient, measuring 11.75 inches overall, weighting less than 30 pounds and requiring less than 450 Watts.

Conclusion

The Scientific Atlanta AVC HD architecture uses at least four TI C64 15 DSPs and multiple Xilinx Virtex FPGAs (with 90 nm technology), delivering unparalleled horsepower required for single-slice HD encoding and for future video quality improvements. The new HD architecture also employs a modular software/hardware design, allowing short-term software up-grades (through downloading new DSP/FPGA code) and/or long-term hardware up-grades (through replacement of cards with others using better and more powerful devices). This innovative HD encoding solution provides a flexible, expandable, versatile HD architecture designed to deliver superior performance for years to come.